Automatic Synthesis of Electronic Circuits using Genetic Algorithms
Síntesis Automática de Circuitos Electrónicos usando Algoritmos Genéticos

Esteban Tlelo Cuautle[1], Miguel Aurelio Duarte Villaseñor[1], Carlos Alberto Reyes García[2] and Gerardo Reyes Salgado[3]

[1]INAOE, Department of Electronics
e.tlelo@ieee.org, miauduvi@inaoep.mx
[2]INAOE, Department of Computer Sciences
[3]CENIDET, Department of Computer Sciences

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Abstract
An automatic synthesis method based on the application of genetic algorithms (GAs) is described for the synthesis of voltage followers (VFs), which are designed using CMOS integrated circuit technology of 0.35μm. It is shown the usefulness of the nullor element to model the ideal behavior of the VF, and to codify its topology using a chromosome which is divided into four genes: gene of small-signal (genSS), gene of synthesis of the MOSFET (genSMos), gene of bias (genBias), and gene of synthesis of current mirrors (genCM); this last one to synthesize ideal current sources used in the biasing of the circuits with CMOS current mirrors.
The proposed synthesis method has been programmed in MatLab, and it uses T-SPICE to evaluate the fitness of the VFs at the transistor level of abstraction. In this manner, the method selects the more appropriated VFs by elitism. Finally, it is shown the behavior of the GA to synthesize practical VFs. As a result, it is shown the synthesis of eight CMOS compatible VFs, and their applications are briefly discussed.
Keywords: Evolutionary electronics, circuit synthesis, voltage follower, nullor.

Resumen
Se describe un método de síntesis automática basado en la aplicación de algoritmos genéticos (GAs) para la síntesis de seguidores de voltaje (VFs), los cuales son diseñados usando tecnología CMOS de circuitos integrados de 0.35μm. Se demuestra la utilidad del elemento anulador para modelar el comportamiento ideal del VF, y para codificar su topología usando un cromosoma que es dividido en cuatro genes: gen de pequeña señal (genSS), gen de síntesis del MOSFET (genSMos), gen de polarización (genBias), y gen de síntesis de espejos de corriente (genCM); este último para sintetizar las fuentes de corriente ideales utilizadas en la polarización de los circuitos por espejos de corriente CMOS.
El método de síntesis propuesto se ha programado en MatLab, y usa T-SPICE para evaluar la aptitud de los VFs en el nivel de abstracción de transistor. De esta manera, el método selecciona los VFs más apropiados por elitismo. Finalmente, se muestra el comportamiento del GA para sintetizar VFs prácticos. Como resultado, se muestra la síntesis de ocho VFs compatibles con CMOS, y sus aplicaciones se discuten brevemente.
Palabras clave: Electrónica evolutiva, síntesis de circuitos, seguidor de voltaje, anulador.

1 Introduction

Nowadays, the design of electronic circuits is accomplished by using a great variety of circuit simulation programs to evaluate their performance before their physical implementation [1]. This design process is well known as computer aided design (CAD). For the case of the design of integrated circuits (ICs), several CAD tools have been developed to perform the automatic synthesis of digital, analog, and mixed-signal circuits [1]-[6]. However, the development of analog CAD tools is advancing very slowly compared to the development of the digital ones. The main reason is that the design of an analog circuit can not be performed from the interconnection of basic cells, as it occurs in the design of digital circuits, where the digital functions are represented with two binary levels, while for an analog circuit all the levels should be considered so that the functions are represented by real numbers. In this manner, it can be appreciated that the automation and development of CAD tools in the digital domain have been matured because the digital design can be performed in a structured process, while analog design does not have regular structures.

Besides, in some circumstances, several analog circuits, such as amplifiers, voltage followers (VFs), and current mirrors (CMs), they can be synthesized automatically [1]-[7].

On the other hand, analog circuit design is much amenable for evolutionary techniques, where contrasting with digital design, there is no solid set of design rules or procedures to automate analog circuit synthesis [2]-[5]. For instance, as stated in [3], if an optimization technique could be found that modified both circuit topology and component values then this could form the basis of an analog synthesis method. Furthermore, Genetic Algorithms (GAs) are just such an optimization technique [8]. GAs operate on the principle of "survival of the fittest", in this manner a GA has the capability to generate new design solutions from a population of existing solutions, and discarding the solutions which have an inferior performance or fitness.

As shown in [2], a GA starts from high-level descriptions to automatically synthesize analog circuits. However, automatic synthesis of analog circuits from high-level specifications is recognized yet as a challenging problem, because the analog IC design process is characterized by a combination of experience and intuition and requires a thorough knowledge of the process characteristics and the detailed specifications of the actual product. Design in the analog domain requires creativity because of the large number of free parameters and the sometimes obscure interactions between them [1]-[7]. Besides, this work introduces guidelines to synthesize practical circuits by applying GAs, and by including rules from the human domain knowledge. The proposed synthesis method begins with high-level descriptions of the analog circuit using nullors [9]-[10], and a refinement process is executed to synthesize CMOS compatible VFs by exploiting the regularity, symmetry, and modularity of the nullor-based descriptions. The proposed GA begins with the creation of random solutions called initial population. Each individual in the population is called chromosome and represents a possible solution to the problem. The chromosome consists of four ordered genes represented by binary strings, and it evolves through iterations called generations. In each generation the chromosomes are evaluated using SPICE to verify their aptitude. The next population is formed by descendents created by combining two chromosomes of the current generation using the crossover and the mutation operators [4]. The synthesized VFs are designed using standard CMOS technology of 0.35μm.

2 VF representation using nullors

The nullor is an ideal element which consists of a nullator (O) and a norator (P) [9]. Furthermore, the ideal behavior of the VF can be represented by using nullators, as shown in Fig. 1 [5],[10]. Each O-element must be joined with a P-element, so that 3 combinations are possible as shown in Fig. 2. Each O-P pair can be synthesized by a MOSFET as shown by Fig. 2(d), where the O-P joined-point is associated to the source (S), the free terminal of the O-element to the gate (G), and the free terminal of the P-element to the drain (D).

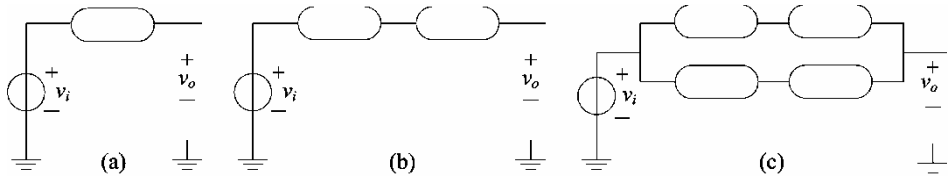


Fig. 1. Modeling the ideal behavior of the VF using nullators

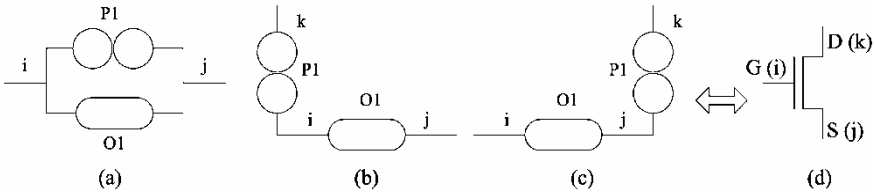


Fig. 2. Addition of a P-element: (a) Between nodes i and j, (b) at node i, and (c) at node j. (d) synthesis of an O-P pair by a MOSFET

Three practical VF topologies by beginning from Fig. 1(c), are shown in Fig. 3. These VFs has been already synthesized in [5], and they are shown herein with ideal biases. The biases can be synthesized further using CMOS compatible CMs as the ones shown in Fig. 4. For instance, in [7] is shown the design and application of a VF which was designed using the VF topology shown in Fig. 3(c) and the CM shown in Fig. 4(a) to synthesize current biases.

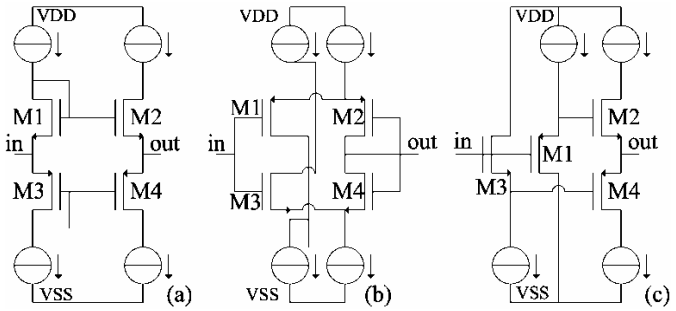


Fig. 3. Synthesis of three practical VFs with ideal biases by beginning from Fig. 1(c)

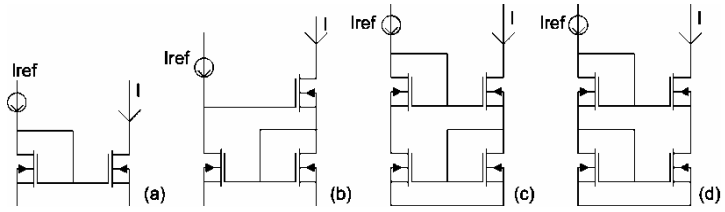


Fig. 4. Current mirrors: (a) Simple, (b) Wilson, (c) Improved-Wilson, and (d) Cascode

3 Genetic codification of the VF

From Fig. 2, the possibilities to add a P to an O-element to form O-P pairs can be represented by a gene of two bits of length (a0a1). This codification creates the gene of small-signal (genSS), which is described in Table 1.
The synthesis of each O-P pair by a MOSFET, as shown in Fig. 2(d), can be represented by a gene of one bit of length (a2). This codification creates the gene of synthesis of the MOSFET (genSMos) to describe the type of transistor, thus when genSMos is '0' the O-P pair is synthesized by an N-MOSFET and when it is '1' by a P-MOSFET.

Each O-P pair should be biased with voltage and current sources, as shown in [5]. The addition of voltage sources is trivial, but the addition of current biases leads to four combinations in each P-element, so that the biasing process can be represented by a gene of two bits of length (a3a4). This codification creates the gene of bias

(genBias), which is described in Table 2. The combination 00 means that the D-terminal of the MOSFET is connected to the most positive voltage (V_{DD}), while a current bias (Iss) is connected between the S-terminal of the MOSFET and the less negative voltage (V_{SS}). The combination 01 means that D is connected to V_{SS}, while a current bias (Idd) is connected between V_{DD} and S. The combination 10 means that a current bias (Idd) is connected between V_{DD} and D, while another current bias (Iss) is connected between S and V_{SS}. Finally, the combination 11 is similar to 10 but by interchanging Iss and Idd.

By using the four kinds of CMs shown in Fig. 4, the synthesis of current biases can be represented by a gene of two bits of length (a5a6). This codification creates the gene of synthesis of CMs (genCM).

Table 1. Codification of genSS

a0	a1	Union	
0	0	Pij	Union point i (Fig. 2a)
0	1	Pi	(Fig. 2b)
1	0	Pj	(Fig. 2c)
1	1	Pji	Union point j (Fig. 2a)

Table 2. Addition of biases to a MOSFET

genBias	Connection	
a3a4	*Drain*	*Source*
0 0	V_{DD}	Iss
0 1	V_{SS}	Idd
1 0	Idd	Iss
1 1	Iss	Idd

As a result, the VF can be codified by using the four genes described above. The length of a chromosome depends on the length of the four kinds of genes. For instance, to codify a VF by beginning from Fig. 1(a), which is related to a one MOSFET circuit, the chromosome consist of seven bits (a0..a6), as shown in Table 3. This means that exist 2^7=128 topologies (candidates) which can be synthesized to generate a practical VF. Besides, GAs can be applied to eliminate those topologies which are not functional, e.g. those in which the input-port or the output-port is connected to V_{DD} or to V_{SS}, as demonstrated in [5]. In the same manner, to codify a VF by beginning from Fig. 1(b) (2 MOSFETs) and Fig. 1(c) (4 MOSFETs), the associated chromosomes grow in number of bits, as shown in Table 3. In this case, genSS is divided by pairs of bits as described in Table 1, genSMos is divided by one bit for each O-P pair to be synthesized by a N-MOSFET or P-MOSFET, genBias is also divided by pairs of bits according to Table 2, and genCM does not change if for Figs 1(a), 1(b), and 1(c), there are only four CMs, e.g. those shown in Fig. 4. It is worthy to mention that the genes can be interchangeable, so that the search strategy is not affected. Furthermore, this new genetic representation improves the one introduced in [10], which requires 25 bits to codify a VF synthesized by 4 MOSFETs, for instance.

Table 3. Number of bits for each chromosome consisting of four genes

VF	genSS	genSMos	genBias	genCM	TOTAL	From Figure
1 MOSFET	2	1	2	2	7 bits	1(a)
2 MOSFETs	4	2	4	2	12 bits	1(b)
4 MOSFETs	8	4	8	2	22 bits	1(c)

4 Intelligent system for the synthesis of VFs

The structure and the steps that execute the proposed intelligent system based on GAs are highlighted in the flow graph depicted in Fig. 5. The GA begins with an initial population called first generation of individuals which is randomly created (spontaneous generation). This generation and the subsequent ones are evaluated three times: the first evaluation selects a correct topology by verifying that neither the input-port nor the output-port of the VF be

connected to either or both V_{DD} or V_{SS}. This first selection does not evaluate a mathematical expression, but it minimizes CPU time since it eliminates the execution of simulations using SPICE for the chromosomes which will not behave as a VF. On the other hand, the second and third evaluations are associated to the fitness functions Vo>k1*Vi and Vo>k2*Vi, where k1 and k2 can be provided by the user and their default value is 0.8 and 0.7, respectively. Basically, the second and third selections are performed using SPICE to calculate the frequency response of the VF and by verifying that the output voltage is between 0.7 and 1.3 volts. Further, an optimization process can be executed to met Vo≈1*Vi to obtain an ideal VF.

As sketched in Fig. 5, the initial population (Generation 1) is passed through a first selection process. The system verifies the topology, so that it discriminates the codes of those chromosomes whose input or output port is connected to V_{DD} or V_{SS}. The selection of a valid topology is accomplished by decoding genSS and genBias, so that if all the individuals have their input or output port connected to V_{DD} or V_{SS}, then it is not necessary to evaluate Fitness1 (Vo>k1*Vi) and Fitness 2 (Vo>k2*Vi), and the system creates a new population. A counter is then incremented to count the number of generations. If at least one individual accomplishes the first selection, that chromosome is a valid topology and the system decodes genSS, genSMos and genBias to generate the SPICE-netlist F1 of the VF topology by adding the CMOS technology. The file F1 includes ideal biases, and it is executed by SPICE to calculate the voltage transfer-function.

A second selection is associated to a fitness function (Fitness 1), which selects all the VF topologies accomplishing Vo>0.8*Vi, where Vo=output voltage and Vi=input voltage. For an ideal VF, Vo=Vi [5]. The SPICE simulation is done by setting Vi=1, so that Vo is plotted by SPICE and the GA verifies if Vo>0.8 at three frequencies: 100Hz, 1KHz, and 100KHz. If any VF is selected, the system eliminates drastically all chromosomes and creates a new population. If at least one VF topology is selected, the system decodes genCM to generate the SPICE-netlist F2 by synthesizing all current biases by CMs from F1. The file F2 is executed by SPICE to calculate the voltage transfer-function.

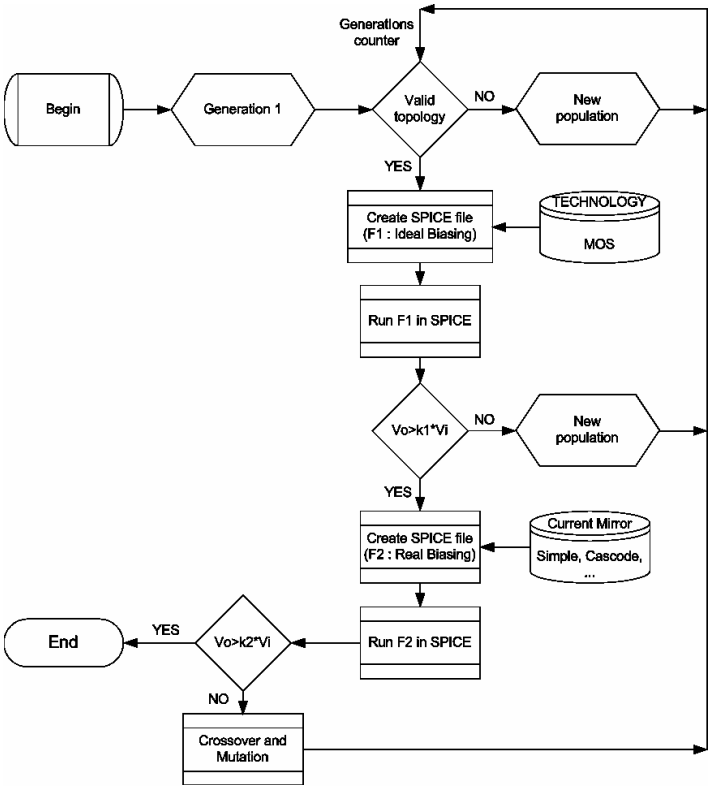


Fig. 5. Flow graph of the proposed synthesis system

A third selection is associated to a fitness function (Fitness 2), which selects all the full-CMOS VF topologies accomplishing Vo>0.7*Vi. Since F1 includes ideal biases, the SPICE simulation of F2 may differ drastically evaluating F1 versus F2. Again, the SPICE simulation of F2 is done by setting Vi=1, Vo is plotted by SPICE and the GA verifies if Vo>0.7 at three frequencies: 100Hz, 1KHz, and 100KHz. If any VF is selected, the system eliminates drastically all chromosomes and creates a new population by applying crossover and mutation operations among the chromosomes in the actual generation. If one CMOS VF is selected, the system finishes its search, i.e. it evaluates by elitism.

An important thing is that if the genes are reordered in Table 3, the mutation operation is not affected since this is a random operation. However, the crossover operation should be modified because this operation combines genes in the parent population with the same significant, e.g. for parents 1 and 2: genSS1 is combined with genSS2, genBias1 with genBias2, and so on. Besides, the reordering of the genes position in a chromosome does not affect the search strategy.

5 Results

The proposed synthesis method has been programmed in MatLab. The fitness functions Vo>k1*Vi and Vo>k2*Vi can be established by the user, and since an ideal VF accomplishes that Vo=1*Vi, the values of k1 and k2 can be between 0.7 and 1.3. Further, an optimization procedure can be executed to tune the value near to the unity. However, Vo=Vi cannot be guaranteed since analog design imposes noise, distortion, gain, bandwidth, impedances and other restrictions [1]. For instance, good VFs can be designed between (Vo/Vi) > 0.98 and (Vo/Vi) <1.02, besides [5].

By setting k1>0.8 and k2 >0.7 to evaluate Fitness 1 and Fitness 2, in Fig. 6 is shown the behavior of the proposed GA by beginning with 30 individuals. In Fig. 6(a) is shown the behavior of the number of individuals. Although from generation 2 to generation 11 the population is constant (4 individuals), the CPU time (normalized) varies as shown in Fig. 6(b). As one sees in generation 2 and 9 the system wasted the high CPU time, but any individual was selected. In Fig. 6(c) is shown the behavior of Fitness 1 and Fitness 2. It can be noted that some individuals passed Fitness 1 (K1>0.8), but they did not pass Fitness 2 (K1>0.7), except at generation 11, where the system finishes its search. In Fig. 7 is shown another execution of the proposed GA by beginning with 20 individuals. Again, the GA holds constant the number of individuals from generation 1 to generation 15. However, the CPU time is different as shown in Fig. 7(b), and the evaluation of Fitness 1 and Fitness 2 is shown in Fig. 7(c).

In Fig. 8 is shown a good behavior of the GA, it begins with 30 individuals and the system finds a solution at generation 4. The population is decreasing as shown in Fig. 8(a), and also the CPU time as shown in Fig. 8(b). In Fig. 8(c) it can be noted that the evaluation of Fitness 2 is better that from Fig. 6(c) and Fig. 7(c).

Finally, the execution of the GA by beginning from Fig. 1(a) generates the four CMOS VFs shown in Fig. 9, in each VF is shown its corresponding binary-chromosome and its corresponding number of combination. In the same manner, by beginning from Fig. 1(b), in Fig. 10 are shown four CMOS VFs along with its corresponding number of combination. In Fig. 11 are shown the SPICE simulation results for the CMOS VFs from Fig. 10, where the chromosome 2567 corresponds to the binary string 101000000111, which is divided into genSS=1010, genSMos=00, genBias=0001, and genCM=11. By beginning from Fig. 1(c), in [5] are shown six CMOS VFs, three of them are shown herein in Fig. 3. In particular the CMOS compatible VF shown in Fig. 3(c) has been used in [7] to design a sinusoidal oscillator. Most important is that a VF can be evolved to design more complex circuits such as current conveyors (CCs), and current-feedback operational amplifiers (CFOAs), as already shown in [11]. In this manner, it is possible to synthesize single resistance controlled oscillators (SRCOs) by applying GAs, as already shown in [6], by using novel difference-differential CCs (DDCCs) which can be designed by combining novel VFs and CMs.

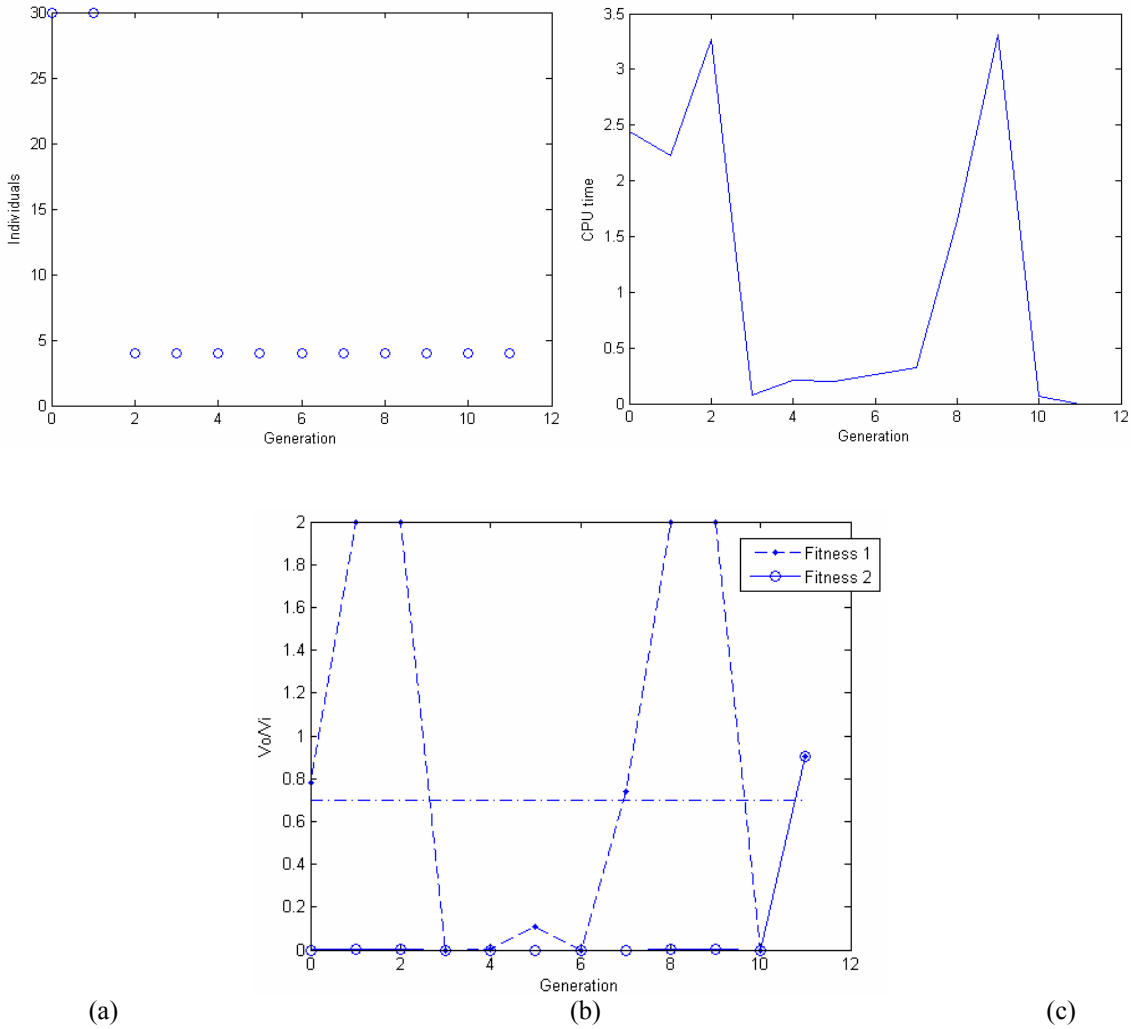
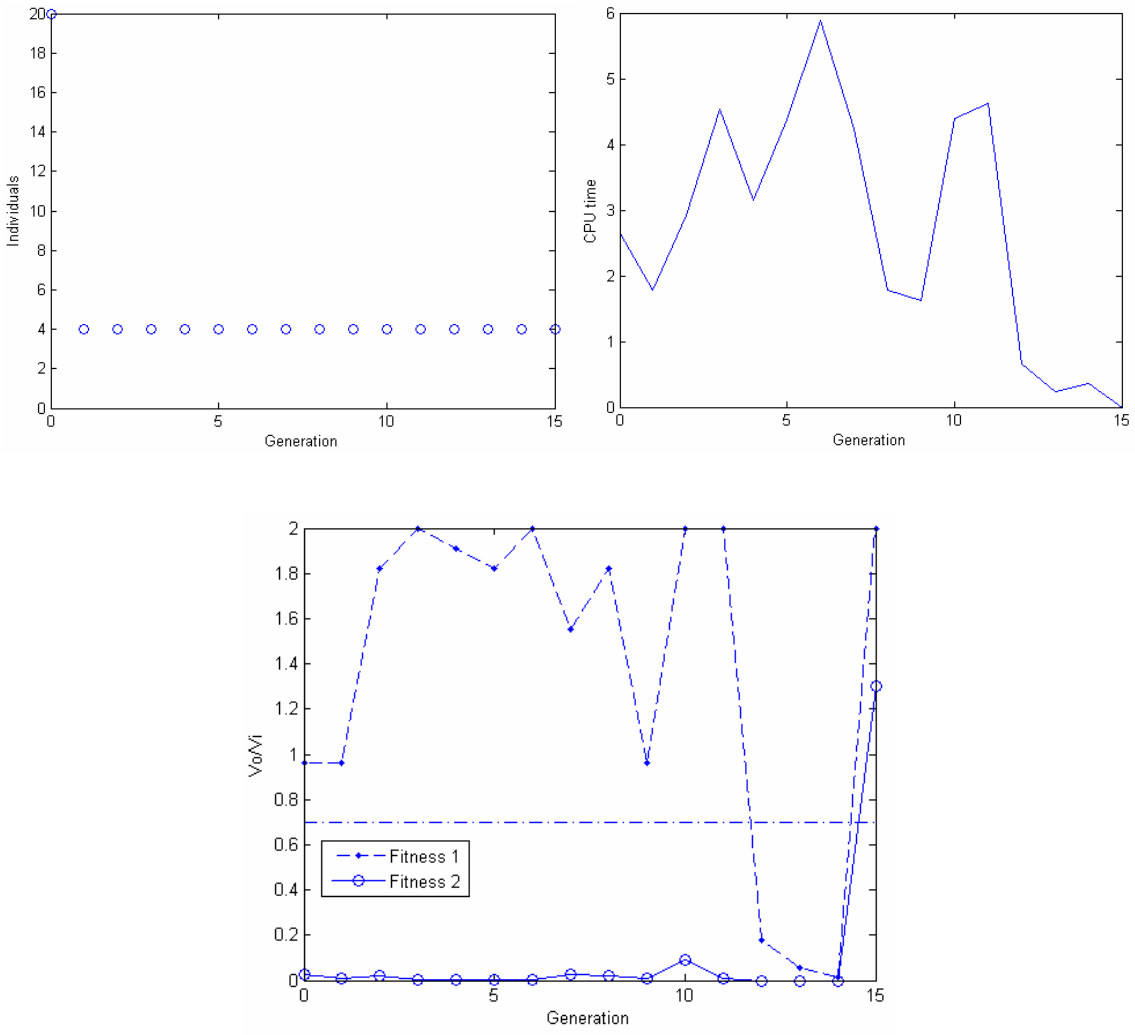


Fig. 6. (a) Number of individuals, (b) Average CPU time, and (c) Evaluation of fitness 1 and fitness 2



(a) (b) (c)

Fig. 7. (a) Number of individuals, (b) Average CPU time, and (c) Evaluation of fitness 1 and fitness 2

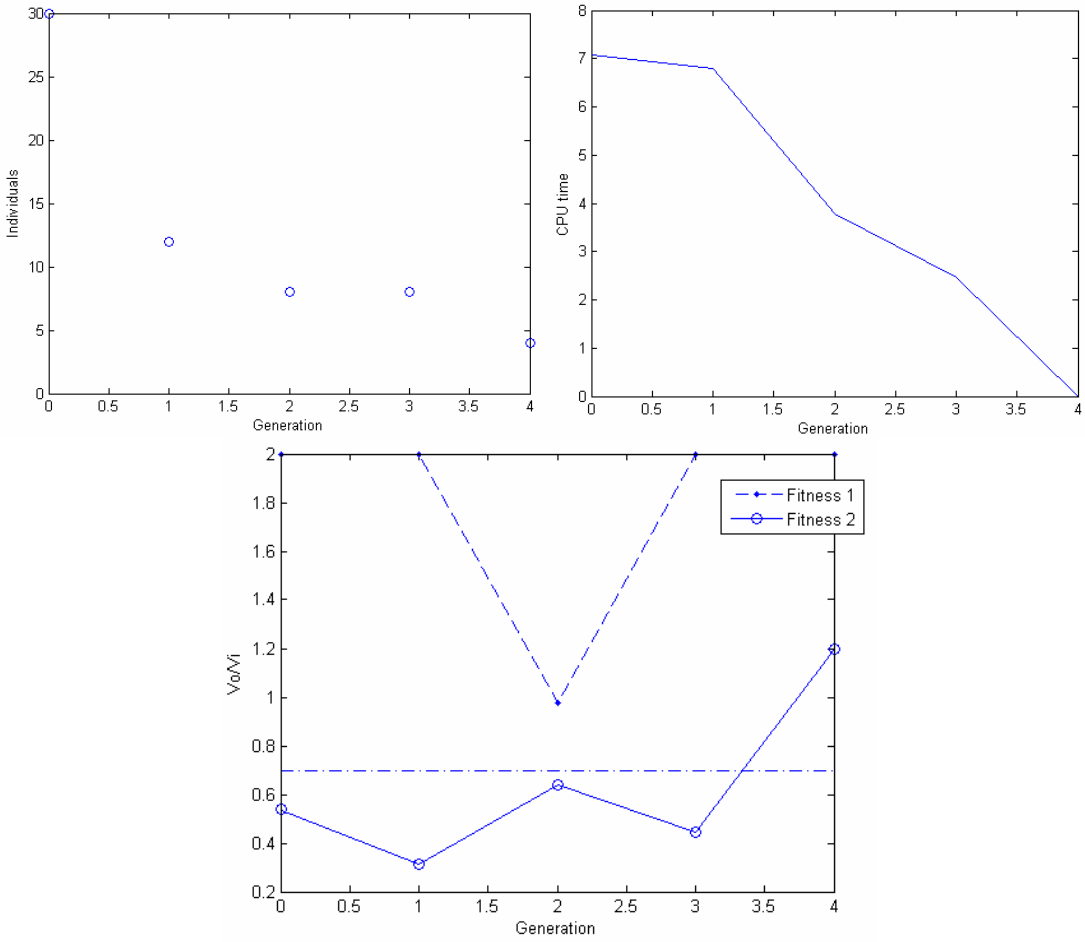


Fig. 8. (a) Number of individuals, (b) Average CPU time, and (c) Evaluation of fitness 1 and fitness 2

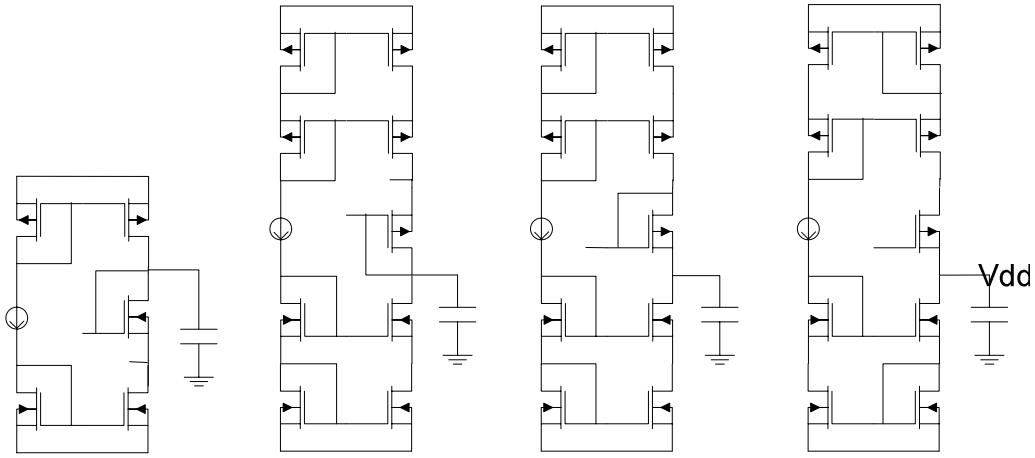


Fig. 9. VF topologies synthesized by beginning from Fig. 1(a)

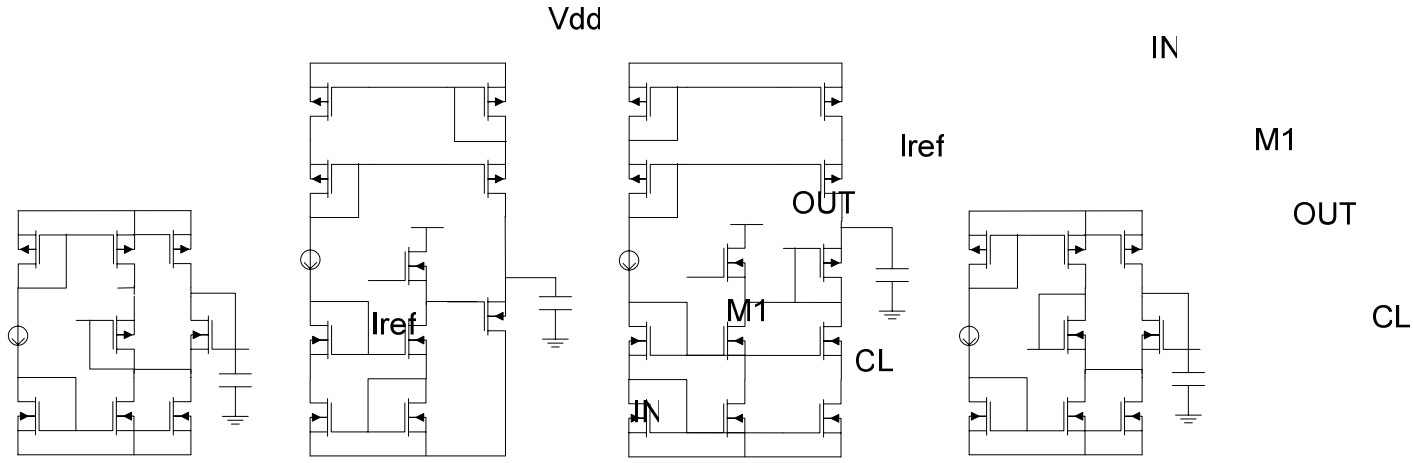


Fig. 10. VF topologies synthesized by beginning from Fig. 1(b)

Vss

0001000
8

Vss

0011101
29

Vdd

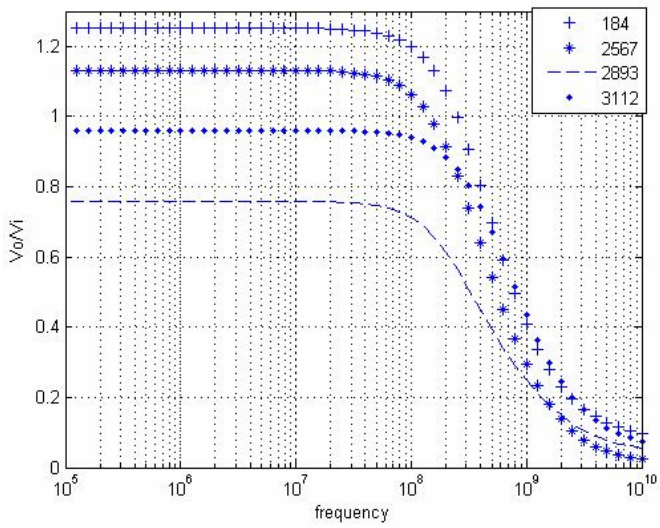


Fig. 11. SPICE simulation results for the VFs shown in Fig. 10. The VFs are associated to the combinations: Fig. 10(a) to 184, 10(b) to 2567, 10(c) to 2893, and 10(d) to 3112

6 Conclusions

It was introduced an automatic system to synthesize VFs by applying GAs. The system was programmed in MatLab, and it interfaces with SPICE to evaluate the behavior of the CMOS VFs by using standard CMOS technology of 0.35µm.

It was proposed a binary codification method (chromosome) to represent a VF by four kinds of genes: gene of small-signal (genSS), gene of synthesis of the MOSFET (genSMos), gene of bias (genBias), and gene of synthesis of current mirrors (genCM). In this manner, the length of the chromosome depends on the length of the four genes. The initial description begins by using nullators (O) to model the ideal behavior of a VF (genSS). Further, each O is connected with a norator (P) to form O-P pairs which can be synthesized by a MOSFET (genSMos). The last step adds current biases (genBias), which are also synthesized by MOSFETs using CMs (genCM). The synthesis process is performed by three evaluations: valid topologies, valid biased topologies (Vo>k1*Vi), and valid CMOS topologies (Vo>k2*Vi). At each evaluation a new population may be created, but the system finishes its search process when a CMOS VF topology accomplishes the third fitness, i.e. when (Vo>k2*Vi). As a result, the synthesis of some new CMOS VF topologies has been shown at the end of this work. An important thing is that the synthesized VFs can be evolved to design more complex circuits such as CCs and CFOAs.

Acknowledgment

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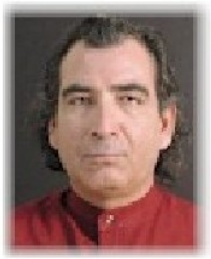
Esteban Tlelo Cuautle *Received the B.Sc. degree from the Technologic Institute of Puebla (ITP), México, in 1993, the M.Sc. and Ph.D. degrees from the National Institute for Astrophysics, Optics and Electronics (INAOE), México, in 1995 and 2000. In 1995 he joined to the ITP, and since January 2001 he is a Researcher at INAOE. He has published over 120 papers on scientific journals and conferences. He is technical editor of the Journal of Applied Sciences, and reviewer of IEEE CAS-I, Education, and Latin America Transactions, Analog Integrated Circuits and Signal Processing, Journal of SCI, ISCAS, ECCTD, WCECS, IASTED and CERMA. His research interests include electronic design automation, modeling and simulation, symbolic analysis and circuit synthesis.*

Miguel Aurelio Duarte Villaseñor *was born in Puebla, México in 1981. He received the Bachelor degree in Electronics from the Faculty of Electronics Sciences (FCE-BUAP), in 2005, and the Master Sciences degree in Electronics from the National Institute for Astrophysics, Optics and Electronics (INAOE), México, in 2007. His research interests include electronic design automation, evolutionary electronics, modeling and simulation and circuit synthesis.*



Carlos Alberto Reyes García *has a C. Sc. PhD degree from the Florida State University. He has a postdoctoral staying at the IIASS in Salerno, Italy. He is a researcher in the C. Sc. Department at INAOE in Mexico. He is a National Researcher Level I at the Mexican SNI. He is the Vice-president of the Mexican Society for Artificial Intelligence (SMIA). He works in; Soft Computing, Speech, Speaker and Infant Cry Recognition.*

Gerado Reyes Salgado *Received the B.Sc. degree from the Technologic Institute of Zacatepec, México, in 1985, the M.Sc. degree from the National Center for Research and Technologic Development (CENIDET), México, in 1995, and the Ph.D. degree from the Institut National Polytechnique de Grenoble (INPG), France, in 2001. He is the Vice-Academic Director at CENIDET, and his research interests include artificial intelligence, cognitive sciences, artificial neural networks, automatic learning, intelligent agents and neuro-symbolic hybrid systems.*